CLAIM LISTING

1. (Original) An electronic circuit adapted to communicate a signal to a plurality of additional electronic circuits over a common transmission line while simultaneously receiving additional signals from the plurality of additional electronic circuits over the common transmission line, the electronic circuit including:

(a) signal sending circuitry coupled to an interface node which is adapted to be coupled to the common transmission line, the signal sending circuitry for applying a signal from the electronic circuit to cooperate in creating a combined signal at the interface node, the combined signal being dependent upon the signal from the electronic circuit and the additional signals simultaneously applied by the plurality of additional electronic circuits connected at other points on the common transmission line; and

(b) decoding circuitry coupled to the interface node, the decoding circuitry for detecting the combined signal at the interface node and decoding the additional signals from the combined signal.

2. (Original) The electronic circuit of Claim 1 wherein the signal sending circuitry includes:

(a) a signal driver; and

(b) an encoding element connected between the signal driver and the interface node.

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3. (Original) The electronic circuit of Claim 2 wherein the encoding element comprises a resistor.

4. (Original) The electronic circuit of Claim 1 wherein the decoding circuitry includes:

(a) a first differential receiver having a positive input connected to receive the combined signal and having an negative input connected to a first reference voltage source.

5. (Currently Amended) The electronic circuit of Claim 1 wherein the decoding circuitry includes:

(a) a reference voltage multiplexer connected to receive a first digital signal as a control signal, and having second and third reference voltage inputs;

(b) a second differential receiver having a positive input connected to receive the combined signal, and an a negative input connected to receive an output of the reference voltage multiplexer.

6. (Original) The electronic circuit of Claim 1 wherein the decoding circuitry includes:

(a) an additional reference multiplexer connected to be controlled by a first digital signal and a second digital signal and having fourth, fifth, sixth, and seventh reference voltage inputs; and

(b) a third differential receiver having a positive input connected to receive the combined signal and an negative input connected to receive an output from the additional reference voltage multiplexer.

7. (Currently Amended) An electronic circuit arrangement including:

(a) a three or more circuits connected together by a common transmission line, each circuit adapted to assert a respective digital signal;

(b) each circuit including sending circuitry connected to the common transmission line, the sending circuitry of the respective circuits cooperating to produce an encoded signal on the transmission line based upon the values of the respective digital signals asserted by the respective circuits, the encoded signal comprising one signal from a set of unique encoded signals with each different signal in the set being representative of a particular combination of digital signals asserted simultaneously from the respective circuits; and

~~(d)~~ (c) each circuit further including a decoding arrangement for decoding the encoded signal appearing on the common transmission line to produce the digital signals asserted from each other circuit.

8. (Original) The electronic circuit arrangement of Claim 7 wherein each circuit is located on a separate integrated circuit chip and the common transmission line comprises a conductor connected to a single electrode on each separate integrated circuit chip.

9. (Original) The electronic circuit arrangement of Claim 7 wherein the signal sending circuitry in each respective circuit includes an encoding element comprising a resistor.

10. (Original) The electronic circuit arrangement of Claim 7 wherein the plurality of circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the second and third circuits includes a first digital signal decoding arrangement comprising:

(a) a first differential receiver having a positive input connected to receive the encoded signal and having an negative input connected to a first reference voltage source.

11. (Original) The electronic circuit arrangement of Claim 7 wherein the plurality of circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the first and third circuits includes a second digital signal decoding arrangement comprising:

(a) a reference voltage multiplexer connected to receive the first digital signal as a control signal, and having second and third reference voltage inputs;

(b) a second differential receiver having a positive input connected to receive the encoded signal, and an negative input connected to receive an output of the reference voltage multiplexer.

12. (Original) The electronic circuit arrangement of Claim 7 wherein the plurality of circuits includes a first circuit providing a first digital signal, a second circuit providing a second digital signal, and a third circuit providing a third digital signal, and wherein the decoding arrangement associated with the first and second circuits includes a third digital signal decoding arrangement comprising:

(a) an additional reference multiplexer connected to be controlled by the first digital signal and second digital signal, and having fourth, fifth, sixth, and seventh reference voltage inputs; and

(b) a third differential receiver having a positive input connected to receive the encoded signal and an negative input connected to receive an output from the additional reference voltage multiplexer.

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13. (Original) An electronic system having a first circuit producing a first digital signal, a second circuit producing a second digital signal, and a third circuit producing a third digital signal, the system including:

(a) a first circuit encoding element included in the first circuit, a second circuit encoding element included in the second circuit, and a third circuit encoding element included in the third circuit, each respective encoding element connected between a digital signal output of the respective circuit and a common transmission network between the first, second, and third circuits, the first, second, and third encoding elements cooperating to produce an encoded signal on the common transmission network based upon the values of the first, second, and

third digital signals, the encoded signal comprising one signal from a set of unique encoded signals with each different signal in the set being representative of a particular combination of the first, second, and third digital signals; and

(b) a first circuit decoding arrangement included with the first circuit, a second circuit decoding arrangement included with the second circuit, and a third circuit decoding arrangement included with the third circuit, the decoding arrangement for each respective circuit for decoding the encoded signal to produce the digital signals produced by each other circuit in the system.

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14. (Original) The electronic system of Claim 13 wherein the encoding elements each comprise a resistor.

15. (Original) The electronic system of Claim 13 wherein the first circuit decoding arrangement includes:

(a) a reference voltage multiplexer connected to be controlled by the first digital signal and connected to receive second and third reference voltage signals as inputs;

(b) a second differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a reference voltage multiplexer output;

(c) an additional reference voltage multiplexer connected to be controlled by the first digital signal and the second digital signal, and connected to receive fourth, fifth, sixth, and seventh reference voltage signals as inputs; and

(d) a third differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the additional reference voltage multiplexer.

16. (Original) The electronic system of Claim 13 wherein the second circuit decoding arrangement includes:

(a) a first differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a first reference voltage signal;

(b) an additional reference voltage multiplexer connected to be controlled by the first digital signal and the second digital signal, and connected to receive fourth, fifth, sixth, and seventh reference voltage signals as inputs; and

(c) a third differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the additional reference voltage multiplexer.

17. Claims 17 and ~~18~~ Canceled

(New) The electronic system of Claim 13 wherein the third circuit decoding arrangement includes:

(a) a first differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive a first reference voltage signal;

(b) a reference voltage multiplexer connected to be controlled by the first digital signal and connected to receive second and third reference voltage signals as inputs; and

(b) a second differential receiver having a positive input connected to receive the encoded signal and a negative input connected to receive an output of the reference voltage multiplexer.